**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-218 (canceled)

219. (currently amended) A chip package comprising:

a ~~preformed~~ substrate comprising semiconductor material;

only one ~~preformed~~ die ~~joined with said preformed substrate~~;

an adhesive material joining said substrate and said only one die;

a first insulating layer comprising a first portion over said only one ~~preformed~~ die and a second portion over said ~~preformed~~ substrate but not over said only one ~~preformed~~ die, wherein said first insulating layer comprises polyimide; and

a first patterned circuit layer over said first insulating layer.

220. (currently amended) The chip package in claim 219, wherein said only one ~~preformed~~ die comprises a first trace formed therein, and wherein said first patterned circuit layer comprises a second trace having a thickness greater than that of said first trace.

221. (previously presented) The chip package in claim 219, wherein said first patterned circuit layer comprises a power bus.

222. (previously presented) The chip package in claim 219, wherein said first patterned circuit layer comprises a ground bus.

223. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer connects multiple portions of said only one ~~preformed~~ die.

Claims 224-227 (canceled)

228. (previously presented) The chip package in claim 219 further comprising a second insulating layer over said first patterned circuit layer.

Claims 229-231 (canceled)

232. (currently amended) The chip package in claim 219 further comprising a second insulating layer on said first patterned circuit layer, and a second patterned circuit layer on said second insulating layer.

Claims 233-235 (canceled)

236. (currently amended) The chip package in claim 219 further comprising a capacitor over said first insulating layer. ~~preformed substrate.~~

Claim 337 (canceled)

238. (previously presented) The chip package of claim 219 further comprising an inductor over said first insulating layer.

239. (previously presented) The chip package of claim 219 further comprising a resistor over said first insulating layer.

240. (previously presented) The chip package of claim 219 further comprising a filter

over said first insulating layer.

241. (previously presented) The chip package of claim 219 further comprising a wave guide over said first insulating layer.

242. (previously presented) The chip package of claim 219 further comprising a micro electronic mechanic element over said first insulating layer.

Claims 243-249 (canceled)

250. (currently amended) The chip package of claim 219, wherein an opening in said ~~preformed~~ substrate accommodates said only one ~~preformed~~ die.

251. (currently amended) The chip package of claim 250, wherein said only one ~~preformed~~ die has a top surface substantially coplanar with that of said ~~preformed~~ substrate.

252. (currently amended) The chip package of claim 219, wherein said ~~preformed~~ substrate comprises a first layer and a second layer, said first layer being on said second layer, an opening in said first layer exposing said second layer and accommodating said only one ~~preformed~~ die.

253. (previously presented) The chip package of claim 252, wherein said first layer comprises a semiconductor material.

254. (previously presented) The chip package of claim 252, wherein said first layer comprises silicon.

255. (previously presented) The chip package of claim 252, wherein said second layer comprises metal.

256. (currently amended) The chip package of claim 252, wherein said only one ~~preformed~~ die has a top surface substantially coplanar with that of said first layer.

257. (currently amended) The chip package of claim 219 further comprising a polymer layer over said ~~preformed~~ substrate and around said only one ~~preformed~~ die.

Claim 258. (canceled)

259. (previously presented) The chip package of claim 257, wherein said polymer layer comprises epoxy.

260. (currently amended) The chip package of claim 219 further comprising a solder bump over ~~on~~ said first patterned circuit layer.

Claim 261 (canceled)

262. (currently amended) The chip package of claim 260 further comprising a gold bump over ~~on~~ said first patterned circuit layer.

263. (currently amended) The chip package in claim 219, wherein said only one ~~preformed~~ die comprises multiple active devices, and said first patterned circuit layer connects said multiple active devices.

264. (currently amended) The chip package in claim 219, wherein said ~~preformed~~ substrate comprises silicon.

265. (previously presented) The chip package in claim 219, wherein said first patterned circuit layer comprises copper.

266. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer is connected to said only one ~~preformed~~ die through an opening in said first insulating layer.

267. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer ~~comprises a first portion~~ over said only one ~~preformed~~ die and across an edge of said only one die. ~~a second portion over said preformed substrate but not over said only one preformed die.~~